## REMARKS

### Status of the Application

Claims 1-12, 14 and 16-21 are pending in the application and have been examined. With this Amendment, Applicant amends claim 20. No new matter has been added.

After entry of this Amendment, claims 1-12, 14 and 16-21 will be pending in the application.

### Objections to the Drawings

The Examiner has objected to the drawings as allegedly failing to show wherein the active device carrying out voltage-current conversion and the active device comprising a negative resistance device are comprised of the same type of transistors ***having electrical conductivities different from each other***, as recited in amended claim 19.

Applicant directs the Examiner's attention to FIG. 11 of the present application, reproduced below, which illustrates "the same type of transistors having electrical conductivities different from each other," as recited in claim 19.

FIG.11

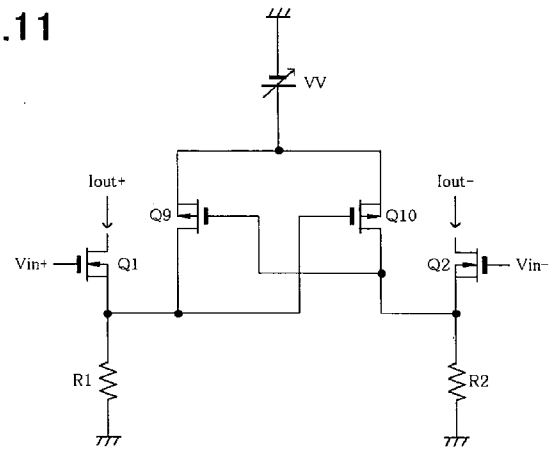


FIG. 11 discloses p-type and n-type metal-oxide-semiconductors (PMOS and NMOS) which are transistors of the same type having electrical conductivities different from each other. The NMOS active device (Q1) carries out voltage-current conversion and the PMOS active device (Q9) comprises the negative resistance device.

Accordingly, Applicant respectfully submits that the drawings illustrate "the same type of transistors having electrical conductivities different from each other" as claimed, and respectfully requests that this objection be withdrawn.

**Claim Rejections**

***Claims 1-12, 14 and 16-21 --- 35 U.S.C. § 103(a)***

Claims 1-12, 14 and 16-21 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,079,443 to Wada *et al.* ("Wada") in view of U.S. Patent No. 6,593,814 to Donig ("Donig"). Applicant traverses this rejection.

Addressing claim 1, the combination of Wada and Donig does not disclose or suggest at least wherein said voltage-controller controls a voltage of said connection node and compensates for voltage fluctuation caused at said connection node by variance of a resistance of said negative resistance device, as recited in the claim. Wada discloses a circuit for supplying a fixed bias voltage to maintain the circuit characteristics even when a resistance of a negative resistance device is changed (see Fig. 6, Q35/R35 and Q36/R36). The Examiner concedes that Wada does not provide the claimed disclosure and relies on Donig to cure the deficiencies. Donig, however, does not provide the disclosure missing in Wada.

Donig provides a regulator circuit which reduces the power supply voltage dropped across an amplifier stage in order to prevent voltage breakdown of the amplifier stage transistors (column 1, line 65-column 2, lines 6). Donig, as cited by the Examiner, discloses a voltage follower circuit which supplies a regulating voltage which varies with power supply voltage to node BK. As disclosed by Donig, a voltage follower in which the potential at the reference node BK follows that of the regulating voltage UR is formed with the regulating loop in the in-phase regulator LR. (column 4, lines 53-57; Fig. 1). ***The regulating voltage UR is linked to the supply voltage potential VCC via the voltage follower in the in-phase regulator LR*** (column 5, lines 4-24). Thus, Donig adjusts the voltage at node BK to allow the use of higher power supply voltages (VCC) without damaging the transistors in the amplifier or requiring transistors with increased voltage breakdown characteristics (column 1, lines 40-47). Accordingly, Donig does not even appreciate the voltage fluctuation issues addressed by the features of claim 1.

On the other hand, in Applicant's claimed circuit, ***the bias voltage compensates for voltage fluctuations at the connection node caused by variance of the resistance of the negative resistance device***.

Further, the Examiner alleges that Wada discloses, *inter alia*, "a voltage-controller (120) electrically connected to a connection node at which said active device and said resistor circuit are electrically connected to each other (node between D20, Q23 and Q24)." Applicant respectfully submits that, as recited by claim 1, the connection node at which said active device (Q1) and said resistor circuit (R1) are electrically connected to each other is placed between Q1 and R1, as shown in, for example, Applicant's FIG. 6. Therefore, the voltage-controller electrically connected to the connection node (between Q1 and R1) is shown in Applicant's FIG.

12 and FIG. 20. This circuit configuration is clearly different from FIG. 2 disclosed by Wada. Accordingly, Applicant respectfully submits that Wada fails to disclose or suggest these features of claim 1.

In view of the above, one of ordinary skill in the art would not have been motivated to combine fixed bias voltage circuitry of Wada with the regulator circuit which reduces the power supply voltage dropped across an amplifier stage disclosed by Donig since the references are not directed to the same issues. Further, even if the references were combined as attempted by the Examiner, the combined references fail to disclose or suggest all of the claimed features.

Accordingly, claim 1 is patentable over the combination of Wada and Donig. Claims 2-10, 12, 14 and 16-19 are patentable at least by virtue of their dependence from claim 1. Amended claim 20 contains features similar to the features recited in claim 1 and is therefore patentable for similar reasons.

Regarding claims 11 and 21, the combination of Wada and Donig does not disclose or suggest at least a voltage-providing circuit electrically connected between a reference voltage point and either a source or an emitter of said field effect transistor or bipolar transistor, and wherein a resistance of said negative resistance device is controlled by controlling a voltage provided by said voltage-providing circuit, as recited in the claim. The Examiner concedes that Wada fails to disclose or suggest these features, and relies on the same circuitry of Donig which was applied in the rejection of claim 1 above to allegedly disclose the claimed voltage-controller for compensating for voltage fluctuations.

As noted above, the circuit disclosed by Donig adjusts the voltage at node BK to allow the use of higher power supply voltages (VCC) without damaging the transistors in the amplifier

(column 1, lines 40-47). Donig's circuit is not connected between a reference voltage point and either a source or an emitter of said field effect transistor or bipolar transistor to control the resistance of said negative resistance device, as required by the claim. Donig also does not disclose controlling the resistance by controlling a voltage provided by the voltage-providing circuit. In other words, the circuit disclosed by Donig is not connected as required by the claim and does not control resistance of a negative resistance device, as required by the claim. Further, the disclosure of Donig does not appreciate the control issues addressed by the claimed features.

It would not have been obvious to ordinary skill in the art to combine the disclosure of Wada with a regulator circuit which reduces the power supply voltage dropped across an amplifier stage disclosed by Donig, since the references are not directed to the same issues. Further, even if the references were combined as attempted by the Examiner, the combined references fail to disclose or suggest all of the claimed features.

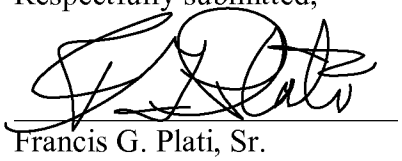
Accordingly, claim 11 is patentable over the combination of Wada and Donig. Claim 21 contains features similar to the features of claim 11 and is therefore patentable for similar reasons.

**Conclusion**

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Francis G. Plati, Sr.
Registration No. 59,153

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